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High-performance low-cost modules with excellent environmental profiles for a competitive EU PV manufacturing industry

HighLite- Deliverable report

D3.3- n-PERT cell with a top efficiency ≥22.5%

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About HighLite

The HighLite project aims to substantially improve the competitiveness of the EU PV manufacturing industry by developing knowledge-based manufacturing solutions for high-performance low-cost modules with excellent environmental profiles (low CO_2 footprint, enhanced durability, improved recyclability). In HighLite, a unique consortium of experienced industrial actors and leading institutes will work collectively to develop, optimize, and bring to high technology readiness levels (TRL 6-7) innovative solutions at both cell and module levels.

HighLite consortium members

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[1] **Deliverable Type**
Please indicate the type of the deliverable using one of the following codes:
R Document, report
DEM Demonstrator, pilot, prototype
DEC Websites, patent fillings, videos, etc.
OTHER
ETHICS Ethics requirement
ORDP Open Research Data Pilot
DATA data sets, microdata, etc.

[2] **Dissemination level**
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Publishable summary

A major and ambitious objective of the HighLite project is to improve the efficiency of low-cost industrial Interdigitated Back Contact (IBC) solar cells from ~23% at the start of the project to ≥24.5% on full-size cells and ≥24.3% on ¼ (or smaller) cut-cell wafers by the end of the project. This requires the implementation of high-temperature passivating contacts, using industrial equipment and a lean process flow, that are compatible with screen-printing metallization. To fast-track developments, competing industrial approaches to form n^+ doped polysilicon-based (poly-Si) passivating contacts are being optimized in T3.3 using n-type Passivated Emitter and Rear Totally diffused (n-PERT) solar cells featuring a boron-diffused emitter at the front and screen-printed Ag contacts on both sides. Industrial approaches for the formation and patterning of n^+ and p^+ doped poly-Si passivating contacts are developed in parallel in T3.4. The most promising approaches will be implemented in low-cost industrial IBC cells also in T3.4 to reach the ambitious IBC cell efficiency targets by the end of the project.

The previous (confidential) report D3.2 (Selection of industrial approaches for high-temperature passivating contacts) reported the results obtained in a round-robin experiment when comparing various poly-Si deposition methods available at the research institutes ISFH, ISC Konstanz, CSEM, imec, CEA INES, and Fraunhofer ISE. It was found that the surface passivation quality of n^+ doped poly-Si contacts differed only marginally between the institutes and more importantly, that negligibly low recombination currents (J_0) were obtained for all contact systems in combination with screen-printing metallization.

In this (public) report, we report on the implementation of n^+ doped poly-Si passivating contacts, formed by ex-situ doped low-pressure chemical vapor deposition (LPCVD), in large area n-PERT solar cells using pilot-production equipment available at imec. We demonstrate efficiencies above 22.5% using a relatively simple process flow. We also show that these high efficiencies levels were obtained by several of the partners involved in T3.3 using different deposition methods to form the n^+ poly-Si. The learnings made in T3.3 are already being used by the HighLite project partners involved in T3.4 to produce high-efficiency IBC cells. In the coming months, the HighLite project partners will continue working on further improving the efficiencies of n-PERT cells with n^+ poly-Si towards 23.5% and beyond while also transferring new learnings made to improve the efficiencies of large-area IBC cells with poly-Si passivating contacts.

Contents

List of acronyms, abbreviations and definitions

Abbreviation	Definitions
Voc	Open circuit voltage (measured at cell level)
IBC	Interdigitated Back Contact
iVoc	Implied Voc (measured before metallisation)
Jsc	Short circuit current
FF	Fill Factor
Eta	Cell efficiency
r_c	Contact resistivity
J_0	Saturation current density. Can be on passivated or on metallised area
ALD	Atomic Layer Deposition
PECVD	Plasma Enhanced Chemical Vapour Deposition
PERT	Passivated Emitter and Rear Totally Diffused
LPCVD	Low Pressure Chemical Vapour Deposition
PL	Photoluminescence
TLM	Transfer Length Method
SDR	Saw Damage Removal
BSF	Back Surface Field

1. Introduction

This deliverable is part of Work Package 3 (WP3) which is entitled "Novel layers and processes implemented in existing solar cell pilot lines". WP3 comprises the following five tasks:

- T3.1: cell manufacturing in pilot lines
- T3.2: Optimization of industrial approaches to minimize cut-edge recombination losses
- T3.3: Optimization of industrial approaches for high-temperature passivating contacts
- T3.4: Implementation of high-temperature passivating contacts in IBC solar cells.
- T3.5: Evaluation of methods for testing and sorting of cut-cells

The approach in T3.3 is to optimize high temperature passivating contacts towards industrial implementation on large area textured substrates (6-inch) with a strong focus on compatibility with low-cost screen-printing metallization solutions. For simplification (no alignment patterning needed) and to avoid issues related to parasitic absorption, n^+ poly-Si passivating contacts are only integrated at the rear side of front-junction bifacial n-PERT cells. Leanings made in T3.3 are being continuously transferred to T3.4 where industrial approaches for the formation and patterning of n^+ and p^+ doped poly-Si layers are being developed to produce high-efficiency IBC cells with passivating contacts.

Deliverable D3.3 is part of T3.3 and follows the previous deliverable report D3.2 (Selection of industrial approaches for high-temperature passivating contacts) which was submitted at M12. Overall, the main objective of D3.3 is to demonstrate a bifacial n-PERT cell with an energy conversion efficiency of at least 22.5% on full-size (6-inch) wafers.

Table 1: Overview of deliverable D3.3.

Deliverable Number	Short deliverable name	Lead beneficiary	Type	Dissemination level	Due date
D3.3	n-PERT cell with a top efficiency ≥22.5%.	IMEC	R	PU	M18

2. Work performed

2.1. Background information

Since decades, the PV industry is dominated by crystalline silicon (c-Si) wafer-based technology. Even if a variety of cell architectures are being manufactured, they mostly rely on the same metallisation scheme with direct contact between the metallization and the c-Si wafer. Despite continuous technological improvements, recombination at the contact regions is becoming nowadays one of the main limiting factors for cell efficiencies to exceed 24%[3].

High-temperature passivating contacts, which incorporate a thin tunnel oxide associated with a heavy doped polysilicon (poly-Si) layer to suppress recombination and promote charge carrier selectivity, offer a promising solution for the race towards high efficiency cells[4,5]. This concept was first introduced in the early 80s for transistor applications. Several approaches for solar cell application were given by Martin Green[6] in the 90s and by Richard Swanson[7] in 2005. A few years later, SunPower was the first company to successfully transfer this technology in their mass-produced IBC cells using a relatively complex process flow featuring copper plated metallization[8].

As of today, most work has been dedicated to integrating these poly-Si passivating contacts in n-PERT solar cells featuring a boron-diffused emitter at the front, n^+ doped poly-Si at the rear, and high-temperature screen-printing Ag metallization on both sides. The industrial viability of different poly-Si deposition methods such as in-situ/ex-situ n^+ doped low-pressure chemical vapor deposition (LPCVD) or in-situ n^+ doped plasma-enhanced chemical vapor deposition (PECVD) available at the research institutes ISFH, ISC Konstanz, CSEM, imec, CEA INES, and Fraunhofer ISE was reported in D3.2.

In this work, the main attention will therefore be focused on an optimization of n^+ poly-Si passivating contacts on large area (6-inch) n-type Czochralski-grown (n-Cz) wafers using an approach based on Low Pressure Atmospheric Chemical Vapour Deposition (LPCVD) and ex-situ n^+ doping in a $POCl_3$ diffusion furnace. The LPCVD system used by imec is a pilot-production tool in which batches up to a few hundred wafers can be processed. Screen-printing metallisation using silver (Ag) pastes fired at high temperatures (700-800˚C) is also selected to meet industry needs for low-cost processing. Finally, the other process steps involved in the cell fabrication, such as p^+ emitter diffusion (in a BBr_3 tube furnace), rear side polishing, wet cleaning, ALD Al_2O_3 emitter passivation, and PECVD SiN_x are also executed in pilot-production tools (with manual loading) in imec's pilot line.

[3] B. Min, M. Müller, H. Wagner, G. Fischer, R. Brendel, P.P. Altermatt, and H. Neuhaus, "A roadmap toward 24% efficient PERC solar cells in industrial mass production." IEEE Journal of Photovoltaics, 7 (2017): 1541-1550.
[4] M. K. Stodolny, M. Lenes, Y. Wu, G. J. M. Janssen, I. G. Romijn, J. R. M. Luchies, and L. J. Geerligs. "n-Type polysilicon passivating contact for industrial bifacial n-type solar cells." Solar Energy Materials and Solar Cells 158 (2016): 24-28.
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[6] M.A. Green. "Silicon solar cells: Advanced principles and practice. 1995." Bridge: Sydney.
[7] R.M. Swanson. "Approaching the 29% limit efficiency of silicon solar cells." In Conference Record of the Thirty-first IEEE Photovoltaic Specialists Conference, pp. 889-894. 2005.
[8] D.D. Smith, G. Reich, M. Baldrias, M. Reich, N. Boitnott, and G. Bunea. "Silicon solar cells with total area efficiency above 25%." In 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), pp. 3351-3355. 2016.

2.2. Results obtained

2.2.1. Optimization of n^+ poly-Si passivating contacts at imec

In the early stage of the project, the first step was to undertake the implementation of the n^+ poly-Si passivating contacts as back-surface field (BSF) in the bifacial n-PERT cell architecture. We addressed a large part of this task by developing a robust n^+ poly-Si formation process using an approach based on ex-situ doped LPCVD. In this approach, a tunnel silicon oxide (SiO_2) layer is grown in-situ (inside the LPCVD tube) using dry oxidation prior to the deposition of an intrinsic a-Si layer (100-200 nm thick) by LPCVD. The process is then followed by an ex-situ phosphorous diffusion in a $POCl_3$ furnace to convert the a-Si layer into n^+ doped poly-Si.

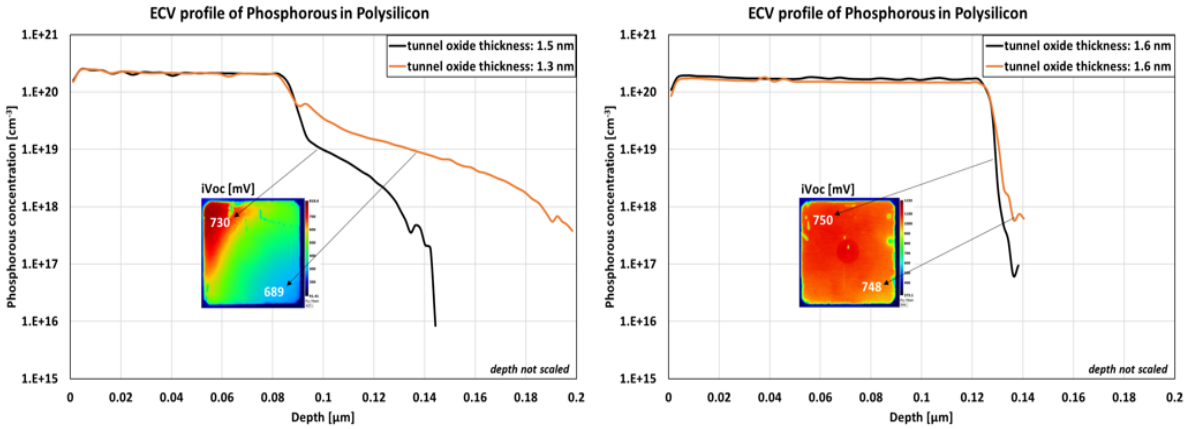


Figure 1. Electrochemical Capacitance-Voltage (ECV) profiles of doped polysilicon for different tunnel oxide thickness. The PL images show the spatial passivation of the 6-inch wafer, with iVoc values at different locations. Note that the x-axis is not scaled.

For this study, we processed symmetrical n-Cz wafers with saw damaged surface (SDR) to mimic the rear of the final solar cell device. The wafers with n^+ poly-Si layers were capped with PECVD SiN_x layers on both sides and characterized by photoluminescence (PL) measurements. Figure 2 shows the impact of the tunnel SiO_2 thickness and uniformity on the PL signal and implied open circuit voltage (iV_{oc}). One can see that insufficient tunnel oxide thickness leads to a strong phosphorous tail diffusion into the Si wafer giving rise to unwanted Auger recombination, as indicated by the lower iV_{oc} values. When the tunnel SiO_2 recipe is optimized in terms of thickness and uniformity, it can act as effective diffusion barrier shown with the Phosphorous concentration dropping sharply at the SiO_2/wafer interface (see right part of Figure 2), giving rise to higher and more uniform iV_{oc} values. In other terms, a more abrupt n^+/n junction leads to a more effective field effect and hence to better selectivity of charge carriers. At this stage, it was therefore concluded that a tunnel SiO_2 with a thickness of at least 1.5 nm was deemed necessary to achieve a good functionality of the passivating contacts. Oxide thicknesses larger than 1.8 nm did not bring any benefit in terms of iV_{oc} but were found to be detrimental for throughputs (due to much longer oxidation times being required) and charge carrier selectivity (due to much higher contact resistance values).

Another feature to look at was the impact of the thermal budget on the active Phosphorous concentration in the n^+ poly-Si layer. This is because the higher the active doping in the n^+ poly-Si layer is, the more abrupt the n^+/n junction can be and the greater the surface passivation between the contacts. Higher n^+ active doping also enables to reduce the saturation current density under the metal contact (J_{0metal}), which in turns further increases V_{oc} values at cell level. High n^+ doping levels within the poly-Si film usually require higher temperatures and/or longer diffusion process time which can be detrimental to the integrity of the thin SiO_2 layer. Indeed, under excessive thermal stress, the tunnel SiO_2 is likely to break locally, resulting in the unwanted phosphorous penetration within the silicon bulk (so called Phosphorous tail). These local breakdowns are directly associated with an electrical leakage that weakens the passivating properties of the n^+ poly BSF and therefore adversely affects the iV_{oc} values. Therefore, to meet the requirement of having a high active n^+ doping level while maintaining a uniform and excellent level of passivation across the wafers, we tested a set of different $POCl_3$ recipes to establish a suitable process window.

To complete the investigation of the n^+ poly-Si passivating contacts, it was also crucial to examine the influence of the same $POCl_3$ thermal budget upon the recombination and resistive losses of the metal contacts applied at the rear of the cells. We therefore coupled and extended the experiment with the analysis of J_{0metal} and contact resistance. For this, a set of sister wafers was processed in parallel with those dedicated for PL mapping. We used a dedicated screen design provided by ISC Konstanz (also used for the work towards D3.2) to print the Ag pastes on the substrates passivated with SiN_x and fired the wafers in a belt furnace. Contact resistance and J_{0metal} values were then extracted using transfer length method (TLM) and PL measurements respectively.

Figure 3 illustrates the results of this experimental matrix. The PL images show a clear degradation of the passivation at higher thermal budget as the tunnel oxide did not sustain the higher temperatures. One can note the transition regime where the SiO_2 breakdown only occurs partially, materialised with iV_{oc} values below 700 mV in the top left corner (green area) of the largest PL image. The data of J_{0metal} revealed values between 100 and 200 fA/cm^2 at the lowest thermal budget for a given Ag paste. Nevertheless, at a lower thermal budget where passivation is uniform with iV_{oc} values around 745 mV after firing, we measured higher contact resistance. This sharp rise is attributed to the fact that the thin tunnel oxide has been integrally preserved when exposed to lower temperatures. Thus, the conduction path of charge carriers via tunnelling effect is hindered as compared to the situation where higher thermal budget creates large leakage paths through the tunnel SiO_2 film.

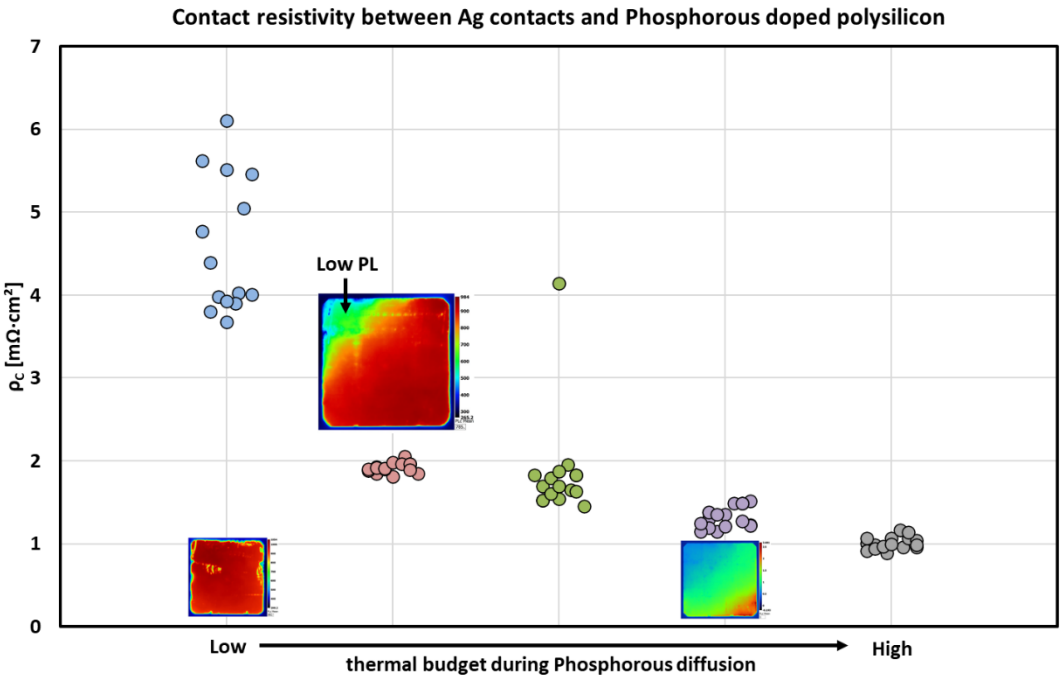


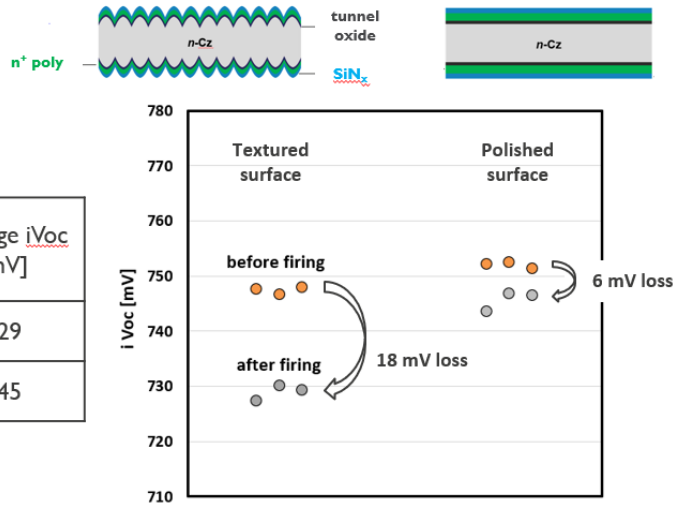
Figure 2. Contact resistivity data as a function of the thermal budget during Phosphorous diffusion. The PL images show the level of surface passivation within the wafer.

These experimental results revealed that the thermal budget during $POCl_3$ diffusion and the SiO_2 thickness are two distinct parameters which converge to the same negative effect if not tuned carefully. They also show how critical the thickness control of the interfacial SiO_2 layer is to the good operation of the cell. A too thin and non-uniform SiO_2 layer strongly undermines the surface passivation properties while a too thick SiO_2 layer leads to high resistive losses between the metal contacts and the wafer bulk.

In addition, we examined the effect of the rear surface preparation upon the electrical quality of the n^+ poly BSF. Structured surfaces such as random pyramid texturing have a significant impact on the adhesion of screen-printed contacts[9]. Indeed, it is desirable to have a reasonably high surface roughness to increase the effective interface area between the silicon wafer and the metal for adherence purposes. This also translates into better electrical cell performance as contact resistance can be strongly reduced[10], which could overcome the detrimental impact of the tunnel oxide regarding carrier transport depicted above. A second reason of having textured surfaces at the rear is that it can help with achieving higher bifaciality values. On the other hand, flat SDR surfaces are generally easier to passivate due to the reduced surface area compared to random pyramid textured surface (factor of 1.7 between flat (100) planes and a textured surface along (111) planes). We therefore compared both types of surface topography, flat SDR and random pyramid textured, to select the best configuration for the n^+ poly BSF.

[9] J. Sergent, "Advanced ceramics and composites" in Book of Ceramics and Composites, New York: McGraw-Hill, 2001.

[10] E.Cabrera. Experimental evidence of direct contact formation for the current transport in silver thick film metallized silicon emittersJournal of Applied Physics 110 (2011)



After firing

surface	Average contact resistivity [mΩ·cm²]	Average J_0 [fA/cm²]	Average iVoc [mV]
textured	2 ± 0.3	6	729
polished	7 ± 5	2	745

Figure 3. The table on the left shows average values of contact resistivity, saturation currents (J_0) of the passivated n^+ poly BSF, and implied V_{oc} (iV_{oc}). The graph on the right shows iV_{oc} before and after firing (3 wafers per group).

As in the previous section, n-Cz wafers were prepared using symmetrical structures, with a stack of SiO_2/n^+ poly-Si, PECVD SiN_x capping, and fired. A first group was metallised with Ag for contact resistance measurements using TLM. In parallel, a second group of wafers was dedicated to J_0 and iV_{oc} characterisation. In both groups, results with polished and textured surfaces were compared. The table in Figure 4 shows the results of contact resistance measurements for both surfaces. As expected, the contact resistivity (r_c) on textured surfaces was found to be much lower than on polished surfaces with tightly distributed values of 2 ± 0.3 mW.cm^2. One the other hand, the r_c values on polished wafers were significantly higher and less uniform at 7 ± 5 mW.cm^2. Locally, we also observed loose Ag contacts which clearly indicates a worse adhesion on flat SDR surfaces. The table and the graph of Figure 4 show the data of J_0 and iV_{oc} before and after firing for both types of surfaces. Although the loss in iV_{oc} is rather limited (6 mV) for polished surfaces, the level of surface passivation is further degraded for textured surfaces, where a loss of 18 mV was measured after firing. While the marginal loss of iV_{oc} before firing can be attributed to the enhanced surface area and greater number of dangling bonds on (111) planes with textured surfaces[11,12,13], the additional loss after firing is likely to be exacerbated by an increase of mechanical stress in the SiN_x-Silicon interface at tips and valleys of the pyramidal structure during the high thermal treatment. Despite this degradation, we shall however underline the excellent level of surface passivation provided by the n^+ poly BSF with J_0 in the passivated areas of 2 fA/cm^2 and 6 fA/cm^2 respectively for flat and textured surfaces. From these results, one can conclude that both surface topographies exhibit their own advantages and disadvantages associated to the passivation properties and series resistance. However, to determine which of the 2 structures may win the race for the highest conversion efficiency, we need to compare them directly at solar cell level.

[11] Ruy S.Bonilla. Dielectric surface passivation for silicon solar cells: a review. Phys. Status Solidi (2017)
[12] K. R. McIntosh, J. Appl. Phys. 105 (2009)
[13] S. C. Baker-Finch, IEEE J. Photovoltaic (2011)

2.2.2. Solar cell process flow at imec

The LPCVD process has the advantages of producing high quality tunnel SiO_2 layers with excellent uniformity (using in-situ dry oxidation) and of creating highly conformal a-Si films. It has however the disadvantage of depositing layers on both sides of the wafers due to their vertical layout in the quartz boat. As a result, the process flow for fabricating the solar cells requires a sequence of masking and etching steps to overcome this problem. The process flow developed at imec starts with random pyramid texturing and p^+ emitter formation (using BBr_3 tube diffusion). As shown in Figure 5, two types of rear side polishing were investigated. A mild polishing (<1 µm Si removed per wafer) to keep the rear side textured and a stronger polishing (>6 µm Si removed per wafer) to get a polished flat rear side. A PECVD oxide mask is then applied at the front side to protect the p^+ emitter during the LPCVD and n^+ poly-Si formation (using $POCl_3$ tube diffusion) processing steps. Another PECVD oxide mask is then deposited on top of the rear n^+ poly-Si BSF to protect it during the subsequent front side n^+ poly-Si etching step in diluted Tetramethyl ammonium hydroxide (TMAH). This chemical has been widely used in microelectronics in the last decades for Si etching due its extremely good selectivity towards SiO_2[14]. The wafers are then cleaned using chemical solutions which also remove the PECVD masks on both sides. Finally, the front (Al_2O_3/SiN_x) & rear (SiN_x) passivation layers are deposited, and metallization is performed on both sides using screen-printing of Ag pastes followed by fast firing in a belt furnace.

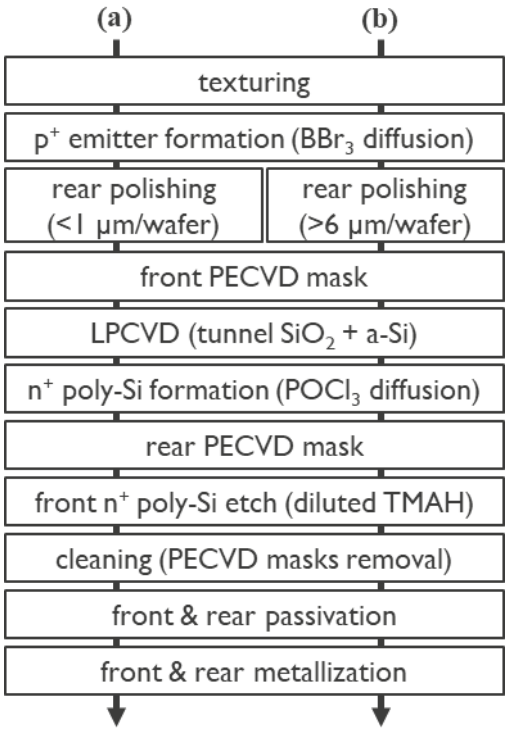


Figure 4. Flow charts for bifacial n-PERT cells at imec with (a) mild rear Si polishing (<1 µm/wafer) to keep the rear side textured and (b) strong rear Si polishing (>6 µm/wafer) to get a flat polished rear side.

[14] O.Tabata. Anisotropic Etching of Silicon in TMAH Solutions. Sensors and Materials, Vol. 13, (2001)

2.2.3. Solar cells results obtained at imec

Front junction bifacial n-PERT cells with n^+ poly BSF were fabricated using 180 µm thick n-Cz substrates with a bulk resistivity of 2 Ω.cm and a surface area of 244.43 cm^2 (M2 format). As mentioned before and shown in Figure 5, both textured and polished rear sides were benchmarked. The screen-printing metallization features a busbarless pattern with screen printed Al/Ag fingers at the front and Ag fingers at the rear. Two different rear Ag pastes (A & B) were tested and compared for 3 different firing conditions. The busbarless cells were measured using a multi-wires GridTouch™ contacting chuck. As in section 2.2.1, separate monitor wafers were processed in parallel for a qualitative and quantitative characterisation of the recombination losses. **As shown in Figure 6, we measured an average cell efficiency of 22.4% for the best 2 groups with 9 cells above the target 22.5% efficiency.** A best cell efficiency of 22.65% was obtained with a polished rear surface.

firing	rear paste	rear surface	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
A	A	textured	39.4	685	79.6	21.5
B	A	textured	39.5	687	79.6	21.6
C	A	textured	39.5	685	79.8	21.6
A	A	polished	40.3	692	80.4	22.4
B	A	polished	40.3	693	80.0	22.3
C	A	polished	40.3	691	80.2	22.3
A	B	polished	40.2	692	80.2	22.3
B	B	polished	40.1	692	80.4	22.3
C	B	polished	40.2	691	80.8	22.4

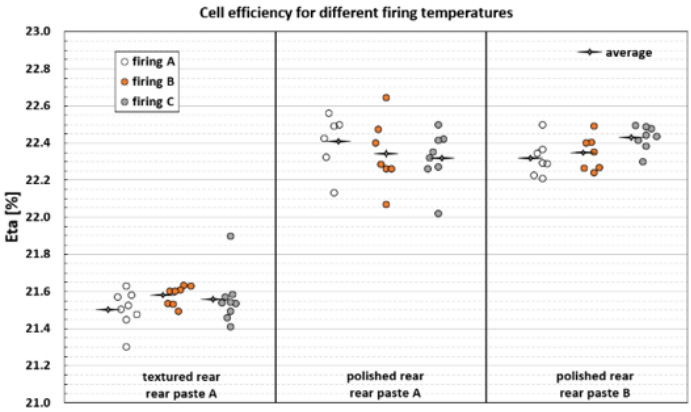


Figure 6. (Left) Average I/V data results and (right) individual efficiency results for all the n-PERT cells processed.

Figure 7 shows the rear contact resistivity (p_c) values that were extracted by TLM for the different rear architectures. Interestingly, one can see that even with p_c values in the range of 5 to 20 mW.cm^2, fill factor values above 80% can easily be attained.

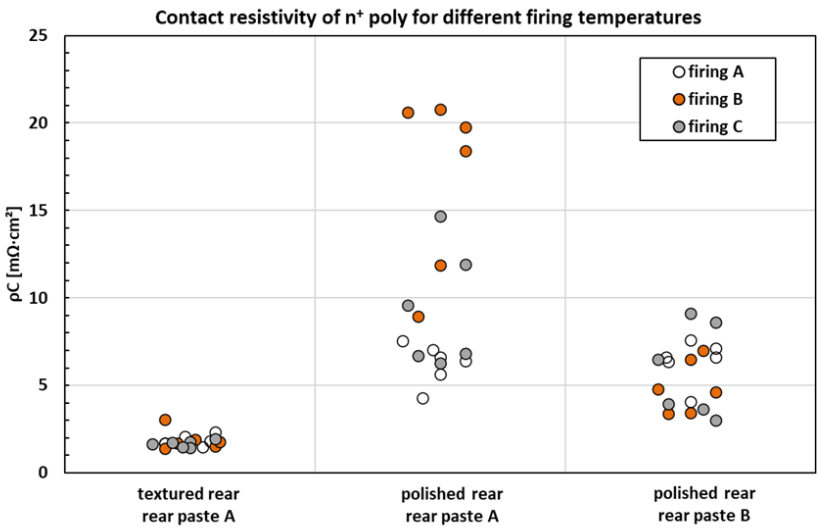


Figure 7. Specific contact resistivity (pc) values measured for the rear architectures, pastes, and firing conditions.

2.2.4. Best cell results obtained by the HighLite partners

With further optimization of the p^+ BBr_3 diffusion, we managed to further improve at imec the efficiency of the best n-PERT cell with n^+ poly-Si passivating contacts to 22.8% mainly thanks to higher V_{oc} values around 700 mV. As shown in Table 2, several other HighLite project partners involved in T3.3 (namely CEA-INES, F-ISE, and CSEM) were also able to achieve efficiencies above 22.5%. Compared to the outstanding 24.9% world-record result for this type of cell, further optimization is required to significantly improve V_{oc}, j_{sc} and FF values. Regarding the V_{oc}, the best results obtained with a homogeneous p^+ emitter appear to be limited to values around ~700 mV due to high recombination losses under the front Ag/Al contacts. Solving this issue will most likely require the implementation of an advanced selective p^+ poly at the front (to drastically reduce contact recombination losses as also proposed for p-PERC cells[15]) which is outside the scope of the work planned in T3.3. Therefore, in the coming months we will focus our attention towards improving j_{sc} and FF values.

Table 2: Non-exhaustive overview of best reported n-PERT cell results with poly-Si passivating contacts and a minimum efficiency of 22.5% obtained on large area (>239 cm²) n-Cz substrates.

Company / Institute	Wafer	TOPCon Technology	Emitter	V_{oc} [mV]	J_{sc} [mA/cm²]	*FF* [%]	*η* [%]
Jinko Solar	n-type, Cz	LPCVD	?	715	41.5 (DARC)	83.8	24.9* [16]
Trina Solar			?	717	40.6	84.5	24.58* [17]
Jinko Solar			?	724	40.7	82.4	24.2* [18]
Jolywood	n-type, Cz	LPCVD	Homo-geneous	705	41.8 (DARC)	82.0	24.1 [19]
MeyerBurger		PECVD		696	41.3 (DARC)	81.0	23.28* [18]
Jolywood		LPCVD		701	39.9	83.0	23.19* [19]
CEA-INES		LPCVD		701	40.4	81.1	23.0* [20]
GCI		?		698	40.3	81.6	23.0 [18]
ISE		PECVD		700	41.2 (DARC)	79.6	22.95* [21]
SERIS		PECVD		696	40.5	80.9	22.8* [22]
IMEC		LPCVD		698	40.4	80.7	22.8
CSEM		PECVD		691	40.7	80.1	22.5 [23]

[15] T. Dullweber, et al. "Evolutionary PERC+ solar cell efficiency projection towards 24% evaluating shadow-mask-deposited poly-Si fingers below the Ag front contact as next improvement step" Solar Energy Materials and Solar Cells, 212, p.110586, 2020.
[16] JinkoSolar, presentation at the N Type c-Si Cell and TOPCon Forum 2020, 3-4 Dec 2020, Changzhou (CN)
[17] https://doi.org/10.1016/j.solmat.2019.110258
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3. Conclusions

As reported previously in D3.2, various industrial poly-Si deposition methods are available to form n^+ poly-Si passivating contacts with excellent carrier selectively. In this report, we have presented results obtained at imec when optimizing an approach based on LPCVD and ex-situ n^+ doping using $POCl_3$ diffusion. We have shown that a careful optimization of (1) the rear surface morphology (textured vs polished), (2) the tunnel SiO_2 recipe (grown in-situ during LPCVD), and (2) the $POCl_3$ diffusion thermal budget is required to achieve excellent J_0, iV_{oc} and p_c values. In addition, we presented a relatively simple process flow to integrate n^+ poly-Si layers in industrial bifacial n-PERT solar cells using industrial tools and conventional screen-printed Ag metallization on both sides. Using this process flow, we demonstrated an average cell efficiency of 22.4% for the best 2 groups with 9 cells above the target 22.5% efficiency. Finally, we demonstrated that several of the HighLite project partners involved in T3.3 were able to demonstrate large area bifacial n-PERT with best cell efficiencies well above 22.5% (with several of those results externally confirmed) using different industrial deposition methods to form the n^+ poly-Si layers.

The learnings made in T3.3 are already being used by the HighLite project partners involved in T3.4 to produce high-efficiency IBC cells. In the coming months, the HighLite project partners will continue working on further improving the efficiencies of n-PERT cells with n^+ poly-Si towards 23.5% and beyond while also transferring new learnings made to improve the efficiencies of large-area IBC cells with poly-Si passivating contacts.