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High-performance low-cost modules with excellent environmental profiles for a competitive EU PV manufacturing industry



HighLite- Deliverable report

D4.2: Demonstrate shingle assembly production tool v1 with a nominal throughput of 4000 full-size cells per hour in dual-line configuration



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About HighLite

The HighLite project aims to substantially improve the competitiveness of the EU PV manufacturing industry by developing knowledge-based manufacturing solutions for high-performance low-cost modules with excellent environmental profiles (low CO_2 footprint, enhanced durability, improved recyclability). In HighLite, a unique consortium of experienced industrial actors and leading institutes will work collectively to develop, optimize, and bring to high technology readiness levels (TRL 6-7) innovative solutions at both cell and module levels.

HighLite consortium members





Document information

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Dissemination level²

PU	Public		
СО	Confidential, only for members of the consortium (including the	Х	
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¹ Deliverable Type

Please indicate the type of the deliverable using one of the following codes: R Document, report DEM Demonstrator, pilot, prototype DEC Websites, patent fillings, videos, etc. OTHER ETHICS Ethics requirement ORDP Open Research Data Pilot DATA data sets, microdata, etc.

² Dissemination level

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Publishable summary

During the first 18 months, AMAT has developed and demonstrated a first version of its shingling equipment based on ECA printing. A second version of the shingling equipment will be developed by month 36.

The first version has the following targets specification:

- Processing of thin (100-160 µm) SHJ cells
- Nominal throughput of 4,000 wph
- Dual lane configuration
- ECA printing is performed on full-size cells
- Reduced overlap: down to 0.5 mm

Thanks to the big effort done in these last 18 months AMAT was able to achieve all these expected specifications.

Additionally, we had to address the increased adoption of larger wafer size in the last years by making several modifications to the tool hardware (HW). In fact, when the proposal was submitted the standard wafer size was 156.75 mm x 156.75 mm (M2 format), but the tool is now able to process up to 166 mm x 166 mm (M6 format) in its current configuration. Further wafer sizes (M12, M10) will be addressed in the next version V2, as we expect their adoption for n-type HJT cells processing will be slightly shifted in time with respect to p-PERC, mainly due to upstream processing equipment availability.

We decided not to implement the inline metrology on this tool (V1) as we preferred to assess the key metrological items in an offline toolset at this stage (including PL, EL, 3D-profilometer), and implement them directly on the final tool. We decided to put more effort in other important tasks, such as enabling 0.5 mm overlap and 120 μ m thick wafer processing.

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